Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method of checking overlap accuracy of patterns on four stacked semiconductor layers, comprising:

forming a first checking pattern on a first semiconductor layer, a second checking pattern on a second semiconductor layer, a third checking pattern on a third semiconductor layer and a fourth checking pattern on a fourth semiconductor layer, wherein the first, second and third checking patterns **in their entireties** overlap to form a first rectangular frame, the fourth checking pattern **in its entirety** is surrounded by the first rectangular frame, a first pair of parallel sides of the first rectangular frame is formed by the first checking pattern, and a second pair of parallel sides of the first rectangular frame is formed by the second and third checking patterns;

measuring overlap accuracy between the fourth checking pattern and the first checking pattern; and

measuring overlap accuracy between the fourth checking pattern and the second and third checking patterns.

2. (Original) The method as claimed in claim 1, wherein the second checking pattern comprises a pair of second parallel line-shaped patterns inside the second pair of parallel sides of the first rectangular frame respectively.

3. (Original)   The method as claimed in claim 2, wherein the third checking pattern comprises a pair of third parallel line-shaped patterns outside the second pair of parallel sides of the first rectangular frame respectively.

4. (Original)   The method as claimed in claim 1, wherein the fourth checking pattern comprises a fourth line-shaped pattern to form a second rectangular frame.

5. (Original)   The method as claimed in claim 1, wherein the first checking pattern comprises two pairs of first line-shaped patterns on the first pair of parallel sides of the first rectangular frame respectively and the two pairs of first line-shaped patterns are parallel.

6. (Original)   The method as claimed in claim 1, wherein the first checking pattern comprises a pair of first parallel line-shaped patterns on the first pair of parallel sides of the first rectangular frame respectively.

7. (Original)   The method as claimed in claim 1, further comprising:

measuring the first checking pattern to obtain a first position in a first dimension;

measuring the fourth checking pattern to obtain a second position in the first dimension; and

checking if the first and second positions fall within a predetermined error range.

8. (Original)   The method as claimed in claim 3, further
comprising:

     measuring the second and third line-shaped patterns on one
side of the second pair of parallel sides of the first rectangular
frame to obtain a first average position;

     measuring the second and third line-shaped patterns on the
other side of the second pair of parallel sides of the first
rectangular frame to obtain a second average position;

     averaging the first average position and the second average
position to obtain a third position;

     overlap scanning the fourth checking pattern on the fourth
semiconductor layer to obtain a fourth position of the fourth
checking pattern along the direction parallel to the first pair of
parallel sides; and

     checking if the third and fourth positions fall within a
predetermined error range.

9. (Original)   The method as claimed in claim 1, wherein the
second checking pattern comprises a second line-shaped pattern on
one side of the second pair of parallel sides of the first
rectangular frame and the third checking pattern comprises a third
line-shaped pattern on the other side of the second pair of
parallel sides of the first rectangular frame.

10. (Currently Amended)   The method as claimed in claim 9, further
comprising:

     measuring the second line-shaped pattern on one side of the

second pair of parallel sides of the first rectangular frame to
obtain a first position X'_{01} of the second line-shaped pattern;

measuring the third line-shaped pattern on the other side of
the second pair of parallel sides of the first rectangular frame
to obtain a second position X'_{02} of the third line-shaped pattern;

averaging the first position X'_{01} of the second line-shaped
pattern and the second position X'_{02} of the third line-shaped
pattern to obtain a third position representing the average
location of the second and third checking patterns;

overlap scanning the fourth checking pattern along the
direction parallel to the first pair of parallel sides of the
first rectangular frame to obtain a fourth position; and

checking if the third and fourth positions fall within a
predetermined error range.

11. (Currently Amended) A method of checking overlap accuracy of
patterns on four stacked semiconductor layers, comprising:

forming a first checking pattern on a first semiconductor
layer, a second checking pattern on a second semiconductor layer,
a third checking pattern on a third semiconductor layer and a
fourth checking pattern on a fourth semiconductor layer, wherein
the first, second and third checking patterns **in their entireties**
overlap to form a first rectangular frame, a first pair of
parallel sides of the first rectangular frame is formed by the
first checking pattern, a second pair of parallel sides of the
first rectangular frame is formed by the second and third checking
patterns, and the fourth checking pattern **in its entirety** is
arrayed as a second rectangular frame and is surrounded by the

first rectangular frame;

measuring overlap accuracy between the fourth checking
pattern and the first checking pattern; and

measuring overlap accuracy between the fourth checking
pattern and the second and third checking patterns.

12. (Original) The method as claimed in claim 11, wherein the
second checking pattern comprises a pair of second parallel
line-shaped patterns inside the second pair of parallel sides of
the first rectangular frame respectively.

13. (Original) The method as claimed in claim 12, wherein the third
checking pattern comprises a pair of third parallel line-shaped
patterns outside the second pair of parallel sides of the first
rectangular frame respectively.

14. (Original) The method as claimed in claim 11, wherein the
second checking pattern comprises a second line-shaped pattern on
one side of the second pair of parallel sides of the first
rectangular frame, and the third checking pattern comprises a
third line-shaped pattern on the other side of the second pair of
parallel sides of the first rectangular frame.

15. (Original) The method as claimed in claim 11, wherein the first
checking pattern comprises two pairs of first line-shaped patterns
on the first pair of parallel sides of the first rectangular frame
respectively and the two pairs of first line-shaped patterns are
parallel.

16. (Original)The method as claimed in claim 11, wherein the first checking pattern comprises a pair of first parallel line-shaped patterns on the first pair of parallel sides of the first rectangular frame respectively.

17. (Original) The method as claimed in claim 11, further comprising:

measuring the first checking pattern to obtain a first position in a first dimension;

measuring the fourth checking pattern to obtain a second position in the first dimension; and

checking if the first and second positions fall within a predetermined error range.

18. (Original) The method as claimed in claim 13, further comprising:

measuring the second and third line-shaped patterns on one side of the second pair of parallel sides of the first rectangular frame to obtain a first average position;

measuring the second and third line-shaped patterns on the other side of the second pair of parallel sides of the first rectangular frame to obtain a second average position;

averaging the first average position and the second average position to obtain a third position;

overlap scanning the fourth checking pattern on the fourth semiconductor layer to obtain a fourth position of the fourth checking pattern along the direction parallel to the first pair of

parallel sides; and

checking if the third and fourth positions fall within a predetermined error range.

19. (Currently Amended)   The method as claimed in claim 14, further comprising:

measuring the second line-shaped pattern on one side of the second pair of parallel sides of the first rectangular frame to obtain a first position X'01 of the second line-shaped pattern; measuring the third line-shaped pattern on the other side of the second pair of parallel sides of the first rectangular frame to obtain a second position X'02 of the third line-shaped pattern; averaging the first position X'01 of the second line-shaped pattern and the second position X'02 of the third line-shaped pattern to obtain a third position representing the average location of the second and third checking patterns;

overlap scanning the fourth checking pattern along the direction parallel to the first pair of parallel sides of the first rectangular frame to obtain a fourth position; and

checking if the third and fourth positions fall within a predetermined error range.

20. (New) A method of checking overlap accuracy of patterns on four stacked semiconductor layers, comprising:

forming a first checking pattern on a first semiconductor layer, a second checking pattern on a second semiconductor layer, a third checking pattern on a third semiconductor layer and a fourth checking pattern on a fourth semiconductor layer, wherein

the first, second and third checking patterns, in their

entireties, define a rectangle, the fourth checking pattern in its

entirety is surrounded by the defined rectangle, a first pair of

parallel sides of the rectangle is defined by the first checking

pattern, and a second pair of parallel sides of the rectangle is

defined by the second and third checking patterns;

measuring overlap accuracy between the fourth checking

pattern and the first checking pattern; and

measuring overlap accuracy between the fourth checking

pattern and the second and third checking patterns.